

What is claimed is:

1. A CMOS image sensor comprising:

a semiconductor substrate having an impurity region
and a gate electrode;

a first spacer formed on a first sidewall of the
gate electrode, wherein the first spacer is overlapped
with a portion of the impurity region;

a second spacer formed on a sidewall of the first
spacer; and

a third spacer formed on a second sidewall of the
gate electrode.

2. The CMOS image sensor as recited in claim 1,
wherein the first spacer, the second spacer and the third
spacer are formed with oxide layers.

3. The CMOS image sensor as recited in claim 2,
wherein the first spacer, the second spacer and the third
spacer are formed by carrying out a thermal oxidation
process.

4. The CMOS image sensor as recited in claim 1,
wherein the impurity region is an N-type.

5. The CMOS image sensor as recited in claim 4,
2 further comprising:
a P-type impurity region formed on the impurity
4 region to provide a photodiode; and
a floating diffusion region spaced away from the
6 impurity region by a predetermined distance.

6. A method for fabricating a CMOS image sensor,
comprising:

a) providing a semiconductor structure, wherein the
semiconductor structure includes an impurity region and a
gate electrode;

b) forming a first spacer on a first sidewall of the
gate electrode, wherein the first spacer is overlapped
with a portion of the impurity region; and

c) forming a second spacer on a sidewall of the
first spacer and a third spacer on a second sidewall of
the gate electrode.

7. The method as recited in claim 6, comprising:

b1) forming a first oxide layer on the semiconductor
structure; and

b2) carrying out an etching process to form the
first spacer.

8. The method as recited in claim 7, comprising
forming the first oxide layer by carrying out a thermal
oxidation process.

9. The method as recited in claim 7, additionally
comprising forming a fourth spacer on the other sidewall
of the gate electrode.

10. The method as recited in claim 9, comprising:

- 2 c1) forming a photoresist pattern covering the
impurity region and the first spacer;
- 4 c2) carrying out an etching process to remove the
fourth spacer;
- 6 c3) removing the photoresist pattern;
- c4) forming a second oxide layer on a resulting
8 substrate; and
- c5) carrying out an etching process to form the
10 second spacer and the third spacer.

11. The method as recited in claim 10, comprising
2 forming the second oxide layer by carrying out a thermal
oxidation process.

12. The method as recited in claim 6, wherein the
2 impurity region is an N-type.

13. The method as recited in claim 12, additionally
2 comprising:

4 d) carrying an ion implantation to form a P-type
impurity region on the impurity region to thereby obtain
a photodiode; and

6 e) forming a floating diffusion region spaced away
from the impurity region by a predetermined distance.

14. A method for fabricating a CMOS image sensor,
comprising:

a) providing a semiconductor structure, wherein the
semiconductor structure includes an impurity region and a
gate electrode formed on a semiconductor substrate;

b) forming a first nitride layer on the
semiconductor structure;

c) exposing the gate electrode and a portion of the
impurity region;

d) forming a first spacer on a first sidewall of the
gate electrode; and

e) forming a second spacer on a sidewall of the
first spacer and a third spacer on a second sidewall of
the gate electrode.

15. The method as recited in claim 14, comprising:

2 c1) depositing a first oxide layer on the
semiconductor structure by carrying out a chemical vapor
4 deposition (CVD);

6 c2) forming a photoresist pattern on the first oxide
layer, wherein the photoresist covers an exposed portion
of the impurity region and the gate electrode;

8 c3) patterning the first oxide layer and the nitride
layer by using the photoresist pattern as a mask;

10 c4) removing the photoresist pattern; and

12 c5) carrying out an etching process to form the
first spacer.

16. The method as recited in claim 14, comprising:

2 e1) forming a second oxide layer on a resulting
structure; and

4 e2) carrying out an etching process to form the
second spacer and the third spacer.

17. The method as recited in claim 14, wherein the
2 impurity region is an N-type.

18. The method as recited in claim 17, additionally
2 comprising:

4 f) carrying an ion implantation to form a P-type
impurity region on the impurity region to thereby obtain
a photodiode; and

6 g) forming a floating diffusion region spaced away
from the impurity region by a length of the gate
8 electrode.